"Fault management method for electronic ballast".

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DESCRIPTION

The present invention relates to the managing of lamp fault conditions in electronic ballasts for one or more gas discharge lamps.

Electronic ballasts include an inverter, typically an half-bridge, for powering gas discharge lamps. The inverter provides a square wave output voltage, which switching frequency is imposed by the lamp controller. The square wave output voltage is processed by a resonant output circuit that provides low current to warm the filaments (high switching frequency), high voltage to ignite the lamps (shift from high to low switching frequency) and a controlled current to power the lamps. Phase sequences and management is driven by the lamp controller.

In electronic ballasts, protection circuits are implemented in order to protect the lamp from damage due to excessive voltage, current, and heat. When a fault condition occurs, the electronic ballast is shut down or shifted to a different mode of operation. Because spurious electrical noise or momentary variation in the lamp current or in the lamp characteristics may be mistakenly interpreted as a lamp fault condition, the electronic ballast would be shut down or shifted to a different mode of operation unnecessarily. Further, if the lamp does not ignite on the first attempt, the status is treated as a lamp fault condition. This fault condition does not consider that lamps under low temperature often ignite after repetitive ignition phases. Existing ballasts address this problem by employing "flasher" type protection circuits that periodically attempt to ignite the lamps. Flasher type circuits provide an indefinite number of ignition attempts and are therefore potentially useful for low-temperature starting. Unfortunately, flasher type protection circuits often produce sustained repetitive flashing in one or more lamps, a characteristic that has proven to be an annoyance to users/occupants. Old lamps are hard to strike too, than

only one strike attempt could be insufficient to ignite the lamp.

In an electronic ballast there is the necessity to detect real fault conditions in different lamp phases (preheating, ignition and running phase). To have a more precision in detection, the protection circuits need a determined sensitivity corresponding to the phases to monitor.

All these additional functions have to be implemented in reduced dimensions and using few external components.

The patent US 5,969,483 discloses a methods for management of fault conditions. It offer immunity to electrical noise and disturbances, and provide multiple ignition attempts for igniting the lamps under low temperature conditions avoiding flashing of the lamps. This method consist in repeating preheating phase and frequency shift, whenever a lamp fault occurs. Because the preheating phase is usually long, the fault management action could be slow.

In view of the state of the art described, it is an object of the present invention to provide a circuit able to avoid the drawback of the prior art.

According to the present invention, these and other objects are attained by means of a method for fault management of electronic ballast for at least one gas discharge lamp comprisesing the steps of: preheating the lamp filaments applying a low current for a predetermined time; igniting the lamp by increasing at a predetermined increasing rate the voltage applied up to a predetermined strike value; characterised by monitoring the lamp current; repeating the steps of igniting the lamp and monitoring the lamp current for a predetermined numbers of times if the lamp current is over a predetermined threshold; powering the lamp at normal operating conditions.

The features and the advantages of the present invention will be evident from the following detailed description, illustrated as a non-limiting example in the annexed drawings, wherein:

Figure 1 shows a diagram of the variation of the frequency of a correct lamp turning on;

Figure 2 shows a diagram of the variation of the frequency in the case a fault of turning on of the lamp;

Figure 3 shows a schematic diagram of an electronic ballast;

Figure 4 shows a schematic diagram of a lamp controller of an electronic ballast;

Figure 5 shows a schematic diagram of a lamp lighting sequence and fault management circuit;

Figure 6 shows a diagram of the behaviour of some signal internal to the lamp lighting sequence and fault management circuit.

Referring now to figure 1, the decreasing rate of the frequency of a correct lamp turning on, is based on the preheating phase at high switching frequency Fpre for a predetermined time Tpre, that is applying a low current to the lamp, followed by the ignition phase, during which the frequency shifts down to the minimum switching frequency Fmin in a predetermined time Tsh, that is increasing at a predetermined rate the voltage across the lamp up to the necessary strike value. When the lamp strikes during ignition phase the lamp is running (normal lamp work).

The proposed method of lamp fault management distinguishes three different fault events: ignition fault; fault during normal lamp work; and lamp removal. Ignition fault means that the system has tried to strike the lamp (with preheating phase followed by a ignition phase), but the lamp has not struck. Fault during normal working means that for any reason a working lamp shuts down. The lamp removal condition implies a new start up of the electronic ballast, so the ballast normal turn on sequence is repeated.

According to the present invention, as is shown in figure 2, at the lamp lightening the lamp controller first warms the filaments driving the half bridge at a fixed and programmable frequency Fpre. This phase (preheating phase) goes on for a time period Tpre which length is programmable.

After that, the lamp controller shifts down the half bridge frequency, at

the frequency Fmin, to attempt to strike the lamp (frequency shift phase), for a time length Tsh programmable.

At the end of frequency shift, the lamp controller checks for lamp ignition, monitoring the lamp current cycle by cycle for a period Tmw. If the peak current is higher than a threshold up to a predetermined number of times, an ignition fault is detected, else the ignition has been successful and the controller drives the ballast in running phase.

In the case of ignition fault the lamp controller tries to re-ignite the lamp up to a predetermined number of times. It means that only the frequency shifting (ignition phase) and monitoring phases are repeated. There is not repetition of the preheating phase. To facilitate the lamp strike the proposed method repeats only the frequency shift and the monitoring phase, because the filaments are still warm. Usually the preheating phase is longer than the ignition plus monitoring phases (typically preheating is 2 seconds long, whereas ignition plus monitoring are 200 msec.); to avoid repetition of the preheating phase permit to speed up the attempt to turn on the lamp.

When the ignition fault has happened up to a predetermined number of time the lamp controller shut off the ballast definitively. So the system does not consume in fault condition.

In the case that lamp ignition happens before the predetermined numbers of faults has been reached, the lamp controller puts the ballast in running phase.

During running phase the controller checks continuously the current cycle by cycle and a running fault is detected, if the peak current becomes higher than a threshold up to a predetermined number of times. So the inverter sequences and fault management are the same as the first lightening case.

The case of lamp removal is treated by the lamp controller like a lamp lightening when a new lamp is set up. Accordingly, the phases sequences and fault treatment are the same as the lamp lightening case.

Figure 3 shows a schematic diagram of an electronic ballast which is adapted for powering at least one gas discharge lamp 35 having a pair of heatable filaments. It comprises a lamp controller 30, which drives a half bridge 33, by means of the outputs HSD and LSD, in turn connected to a resonant output circuit 34 and therefore to the lamp 35. The lamp controller 30 has two terminals OSC and CT to which are connected respectively two capacitors Cosc and Ct, used for an oscillator and a timing circuit internal to the controller 30. The electronic ballast further comprises a power supply circuit 31 and an self supply circuit 32 which provide a supply voltage to the lamp controller 30 at the terminal VCC. It also comprises a current detection circuit 36 which provide a signal to the terminal CS of the lamp controller 30; and a no-load detection circuit 37 which provide a signal to the terminal NLD of the lamp controller 30. The electronic ballast circuit is well know to the skilled in the art and will not be explained in detail.

The method according to the present invention it is implemented in the lamp controller 30 and an exemplary schematic embodiment of it is shown in figure 4. It comprises a supply control 43 which supply all the circuits shown in figure (the connections are not shown). There is a controlled oscillator 44 with the terminal Osc connected to the capacitor Cosc which determine the oscillator frequency. It receive the signals Brun (begin running), Bign (begin ignition) and Bpre (begin preheating) and provide as output the signal Fswitch connected to a control logic 42 which in turn drive the driver 41 providing the output HSD and LSD which drives the half bridge 33. The control logic 42 receives also as input a signal SD (shout down), an input NLD (no load detection) and provide as output a signal RS (reset). The circuit related to the lamp lighting sequence and fault management have the reference number 45. The lamp lighting sequence and fault management circuit 45 comprises a sensing circuit 47 having as input a signal CS provided by the current detection circuit 35 and output signals Fign (fault ignition) and Frun (fault running) which are provided to a

protection circuit 48. The protection circuit 48 receive as input also the signals RS, Brun, Epre (end preheating), ED and Bwind (monitoring window), coming from a phase timing circuit 46. The protection circuit 48 provide as output the signal SD, provided to the control logic 42, the signals Bpre, Bign, DISCHARGE, provided to the timing circuit 46. The timing circuit 46 receives further the signal RS, and has a terminal CT to which is connected the capacitor Ct.

Figure 5 shows a schematic diagram of the lamp lighting sequence and fault management circuit 45.

Two current generators Ipre and Iign controlled respectively by the switches S1 and S2 charge the capacitor Ct that can be discharged by the transistor T controlled by an or circuit 50. The capacitor Ct is connected to the input of 4 comparator 51-54, which respectively compare the voltage Vct of the capacitor Ct with respectively the prefixed references voltages Vp, V0, Vi and Vr. The reference voltages Vp, V0, Vi and Vr represent respectively: Vp the end of the preheating phase; V0 the end of discharging Ct; Vi the end of the ignition phase and Vr the beginning of running phase (see fig.6).

Two others prefixed references voltages Thign and Thrun are applied to two comparators 55 and 56 which compare them with the voltage coming from the terminal CS that is coming from the current detection circuit 35 and it is an indicator of the current in the half bridge circuit 33. The signal Epre at the output of the comparator 51 is connected to a S input of a SR flip flop 57, the signal Bign at the output Q and the signal Bpre at the inverted output Q of it, control respectively the switches S2 and S1. The signal Bign is also applied to a pulse circuit 58 which provide at it output a signal which is applied to an or circuit 59. The or circuit 59 receive as input also the signals REPEAT and RESTART. The output of the or circuit 59 is applied to a S input of a SR flip flop 60 which output Q produce a signal called DISCHARGE which is connected to an input of the or circuit 50, the other

input of it receive the signal RS that is the general reset coming from the circuit 43. At the R input of the SR flip flop 60 is applied the signal ED coming from the comparator 52. At the R input of the SR flip flop 57 is applied the output of an or circuit 61 which receive as input the signals RS and RESTART.

The comparator 53 provide a signal Bwin which is applied to an exclusive or 62 together the signal Brun provided by the comparator 54, and provide as output a signal Mwin (monitor window) which is applied to an input enable of a counter n1. The signal Bwin together to the signal coming from the comparator 55 are applied as input of an and circuit 63 which output is connected to the in input of the counter n1. At the input clear of the counter n1 is applied the signal at the output of an or circuit 66; the output of the counter n1 provide the signal REPEAT. The output of the comparator 56 together to the signal Brun are applied to an and circuit 64 which provide as output the signal Frun which is applied together to the signal REPEAT to a switch S3 controlled by the signal Brun. If Brun is high pass through the signal Frun, if Brun is low pass through the signal REPEAT. Such a signal is applied to the in input of a counter n2, at the input enable is applied the signal Bwin. The signal Brun is also applied to a pulse circuit 65 which output together the signal RS are applied to an or circuit 66 which output is connected to the clear input of the counter n2. The output of the counter n2 is applied a switch S4 controlled by the signal Brun. If Brun is high the signal at the output of S4 is considered to be the signal RESTART, if Brun is low the signal at the output of S4 is considered to be the signal SD (shout down).

Figure 6 shows a diagram of the behaviour of some signal internal to the lamp lighting sequence and fault management circuit 45. In particular the variations of the voltage Vct at the terminal of the capacitor Ct varing some signals of the fault management circuit as Bpre, Bign, DISCHARGE, REPEAT and RESTART.

At the start up of the circuit, the reset pulse RS clears the counters, it assures Ct is discharged and it resets flip-flop 67: the signal Bpre (beginning of the preheating phase) is set high. Switch S1 is turned on and the current generator Ipre charges the capacitor Ct up to Vp.

Preheating goes on for period Tpre (see fig.6), during which the half bridge works at fixed preheating switching frequency, to warm the filaments.

When Tpre ends (Ct voltage is up to Vp), the signal Epre (end of preheating) goes high and sets (flip-flop 67) the signal Bign (beginning of the ignition): the igniyion phase starts. Switch S1 is turned off, while switch S2 is turned on. The current generator Iign charges Ct, previously discharged by signal DISCHARGE. Signal DISCHARGE is set high by flip-flop 60 at the beginning of ignition phase. The set pulse of flip-flop 60 is a pulse corresponding to the rising edge of signal Bign and it is produced by the circuit pulse 58. Ignition phase ends when Ct voltage is up to Vi.

During ignition the switching frequency shifts from preheating switching frequency down to minimum switching frequency (frequency imposed for running). The frequency sweep goes on for period Tsh (shift time): the minimum frequency is reached when Ct voltage is up to Vi.

The charging of Ct from Vi to Vr determines by xor gate 62 a time window (Tmw, corresponding to Mwin signal), to monitor lamp current at minimum switching frequency. The lamp current reading occurs cycle by cycle and the information about it is the voltage drop on resistor Rsense (see figure 3). This information is brought to pin CS. If cycle by cycle lamp current is higher than maximum ignition current level during monitor window Tmw, the voltage drop on resistor Rsense, Vsense (at pin CS, figure 3), is up to ignition threshold Tign. It means the lamp does not strike yet, even if the frequency sweep is completed. So comparator 55 output Fign (fault in ignition) goes high. Counter n1, which is enabled during monitor window Tmw, counts Fign pulses. When n1 Fign pulses occur in Tmw,

counter n1 gives REPEAT pulse output, to discharge Ct and to repeat the ignition phase (frequency shift Tsh and monitor window Tmw). Counter n2, enabled at the beginning of the monitor window (Bwin) and active during monitor window and running phase, receives as input REPEAT pulses; switch S3 switches REPEAT pulses to counter n2 input during Tmw, that is before running phase starts (Brun, beginning of running, low). When n2 REPEAT pulses occur, counter n2 gives as output SD pulse (shut down pulse); it is because switch S4, in correspondence to S3, switches the counter n2 output to SD wire (Brun low). It means if n2 REPEAT pulses occur, the lamp has no more chance to attempt ignition and the ballast controller is shut down.

If lamp strikes during ignition phase, the running phase starts when Ct voltage reaches reference voltage Vr: the signal Brun (beginning of running) goes high. Switch S3 switches comparator 56 output to counter n2 input and switch S4 switches counter n2 output to RESTART wire. Counter n1 and counter n2 are reset by a pulse corresponding to the rising edge of signal Brun. If during running phase the lamp current is higher than the maximum allowed running current, sense voltage Vsense (at pin CS) is up to run threshold Thrun and comparator 56 output Frun (fault in running) goes high. If sense voltage Vsense is up to Thrun n2 times, counter n2 gives a RESTART pulse and the circuit repeats the start up phases sequence:. preheating phase, ignition phase (shift phase and monitor window).